Design and test of nonlinear Class-E and Class-F RF power amplifiers

José Ricardo Casallas
Universidad Santo Tomás
Tunja, Colombia
jcasallas@ustatunja.edu.co

Nestor Peña Traslaviña
Universidad de Los Andes
Bogotá, Colombia
npena@uniandes.edu.co

Abstract. **RF power amplifiers of high efficiency and low consume are very important for applications where the size of the device is important, such as mobile phones, network sensors or PDAs. The classical operation modes as Class-A, Class-B and Class-AB amplifiers have a good linearity but a low efficiency, in contrast, Class-E and Class-F amplifiers are not linear, but they present a higher efficiency. In this paper, we present a methodology for designing and building no-lineal microwave and RF power amplifiers. To build the amplifiers we propose the use of transmission-lines, that facilitate the practical implementation because of the low availability of a wide range of lumped elements in the market but they can be replaced by transmission-lines.**

Index Terms— Amplifier Design, RF. *Transmission-lines.*

I. INTRODUCTION

In applications such as mobile communications, low power amplifiers, low noise amplifiers, amplifiers for wireless networks, etc. where the size of the devices is an important requirement, it is necessary to have maximum efficiency amplifiers.

Classical amplifier operation modes like Class-A, Class-B and Class-AB, are characterized by good linearity but low efficiency. In many cases, linearity is a critical specification to be met, but higher power and efficiency means strongly nonlinear behavior. Depending on the application and modulation type, the design of the RF power amplifier can trades the linearity for efficiency and power output. These applications include systems that can tolerate high levels of amplitude distortion such as those using FSK and GMSK.

Class-E and Class-F amplifier operation modes belong to the classification of non-linear amplifiers. In the amplifier operation mode Class-E, the sinusoidal output signal is obtained through a tuning circuit which can be a load capacitor in parallel or a parallel circuit that extracts the fundamental component of the switching signal that transistor delivers [2] [3] [4] [5]. In the amplifier operation mode Class-F, the active device acts as a current source (saturation) [2] [6] [7].

We present a methodology for the design and manufacture of non-linear power amplifiers; we achieve optimum design following a process of a few specifications.

The paper is organized as follows. Part 2 presents basic concepts, section 3 presents the proposed methodology for the design and manufacture of non-linear amplifiers, and some of the designs and experimental results obtained. Finally in Section 4 shows the findings of the investigation.

II. THEORETIC CONCEPTS

A. *Power Amplifier: Efficiency*

For power amplifiers, there are three main concepts of efficiency: Drain efficiency, Power Added Efficiency (PAE) and overall efficiency [8]. Drain efficiency (η) is the ratio of RF output power (Po) to the DC power input ($P_{IN,DC}$):

$$\eta = \frac{P_O}{P_{IN,DC}} \quad (1)$$

The Power Added Efficiency (PAE) is the ratio between the difference of output power (Po) and RF (P_{IN}) to the DC power ($P_{IN,DC}$):

$$PAE = \frac{P_O - P_{IN}}{P_{IN,DC}} \quad (2)$$

The overall efficiency (EFF) is the ratio between the RF output power (Po) and the RF input power (P_{IN}) plus DC power ($P_{IN,DC}$):

$$EFF = \frac{P_O}{P_{IN} + P_{IN,DC}} \quad (3)$$

B. *Non-linear amplifiers: Class-E and Class-F*

Non-linear amplifiers or tuned are those which do not linearly amplify an input signal, but use a switching transistor and a filter circuit that eliminates the harmonics providing a sinusoidal output.

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Class-E mode amplifier operates as a switch with a load network that models or shapes up the output signals, on the active device, current and voltage, in order to avoid that these signals occur simultaneously to minimize power dissipation, especially during switching transitions. In the ideal situation, the efficiency of a class-E amplifier is 100%. However, in practice, the switch has a finite on-resistance, and the transition times from the off-state to the on-state are not negligible. Both of these factors result in power dissipation in the switch and reduce the efficiency.

The efficiency is maximized by minimizing the dissipation in the device, while delivering the desired output power. In RF power amplifiers most of the power dissipation occurs in the power transistor. Specifically, it is the transistor voltage multiplied by the current at each point in time during the RF period integrated and averaged over the RF period [1].

The Class-F amplifier is a type of amplifier that can provide major improvements in terms of power and efficiency. In this amplifier, the device acts as a current source (saturation). It seeks to replace the device in the output waveform by a square wave sinusoidal periodical. Efficiency is achieved by using harmonic resonators in the output network to shape the waveforms of the collector or drain and make them as close as possible to a square wave to a voltage signal and corrected for the current. [6] [7] [9].

III. PROPOSED METHODOLOGY

A. *Overview*

A design methodology is in general a sequence of stages. The first two seek the selection of the appropriate active device taking into account some fixed design parameters. Once the device has been selected then there is a step where analytically the optimal parameters of the load network are calculated. The circuit design is implemented with ideal lumped elements, seeks to maximize the gain and power efficiency. The next stage is done by matching the 50 Ω input characteristic impedance of. Finally, the ideal elements are replaced, step by step, by the actual elements and lumped elements by transmission lines.

B. *Stage 1: Design parameters, selection and characterization of the active device*

The purpose is to identify and adequately characterize the active device. This selection depends on the type of application and can be: BJT, FET, NMESFET, LDMOSFET or HBT [6].

The main parameters that should be calculated in the active device are: (1) saturation voltage to a level of load current, (2) capacitance of the output device and (3) of the transistor electrical parameters such as maximum power, maximum voltage "drain-source" (Vdsmáx), Max "drain-source" (Idsmáx), maximum voltage "gate-source" (Vgsmáx) and frequency. The steps to calculate these values are the following:

Step 1: Define the design parameters: output power, operating frequency and power supply.

Step 2: Select the transistor. The characteristics of the device, power, electrical parameters and frequency are defined from the specifications of the amplifier and the design equations; it is very important to take into account the availability in the market.

Step 3: Obtain the saturation voltage. This is achieved by means of the VI curves for the load current required.

Step 4: Obtain the output capacitance.

You can use the models available in the literature (Spice, etc.), or calculate them by means of the S parameters, through precise measurements of small signal under different conditions of polarization and a wide frequency range. In this case, we must transform the parameters to S parameters and impedance Z and admittance to describe the electrical behavior through a nonlinear model in the form of an equivalent circuit with nonlinear parameters [3] [9].

C. *Stage 2: Calculation of the analytical parameters of the load network*

The aim is to maximize the efficiency of the collector and harmonic suppression necessary for the characteristics of the output power, voltage and output capacitance of the device given.
To select a topology, we must take into account voltage power supply and operating frequency. Different topologies for amplifiers switched class-E and Class-F have been proposed in the literature, among others there are:

- Class-E with shunt capacitance [3]
- Class-E with parallel circuit [12]
- Class-E with transmission lines [3] [12] [13]
- Class-E with quarter-wave transmission line [3]
- Class-F and inverse Class-F [6] [7] [9]
- Class-F with harmonic suppression using ESB (electromagnetic stop band) - DGS (Defected ground structure) [15] [16]

These networks provide good results; for the design shown in figure 1, it was used a Transmission-Line Load-Network Topology [4] [5] [12] [13], because it facilitates that the components of the amplifier can be estimated more accurately using the design methodology presented. The figure below shows the basic topology.

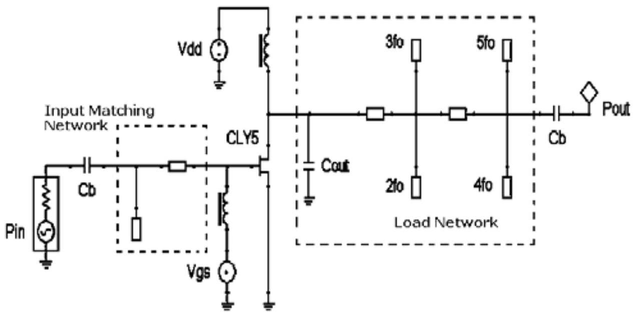

Fig. 1. Transmission-Line Load-Network Topology.

In this configuration we calculated the parameters of the network load by means of the equations presented by Raab [12]. Then we transformed the load impedance (50Ω) to the optimum impedance calculated by means of two transmission lines and transmission line open circuit "stubs", which also provide the necessary harmonic suppression.

D. Stage 3: Selection bias circuit:

The purpose of this stage is to ensure proper polarization networks to optimize the current of operation and minimize the effect of variations in temperature to maximize the gain of power and power added efficiency (PAE)[9].
Bias circuits are different for different types of active devices that can be used in the power amplifier, for instance BJT, FET, NMESFET, LDMOS and HBT [3].

E. Stage 4: Design of matching networks

The purpose of this stage is to minimize the return loss. The input matching circuit must ensure that the return losses are minimal, to ensure maximum power gain, the maximum aggregates power efficiency and stable operating conditions. Once you have the output network the input matching circuit can be done, using well known methods of matching impedance.

F. Stage 5: Optimization of the final circuit

The purpose of this stage is the optimization of the parameters of the circuit to minimize losses and maximize efficiency. Component values of the blocks forming the amplifier are optimized according to the characteristic that they affect by minimizing or maximizing the value.

G. Stage 6: Transformation to layout to manufacturing

When the results have been achieved in the simulations, the load network can be transformed to a microstrip circuit for practical realization. Figure 2 shows the schematics of a complete amplifier in operation mode Class-E.

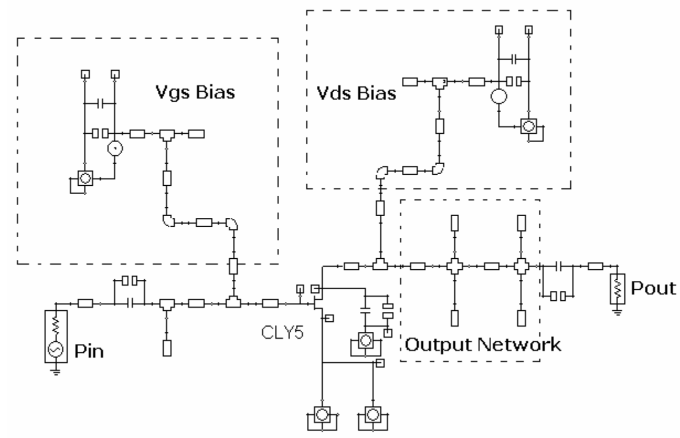

Fig. 2. Class-E amplifier schematics.

In this circuit we can see the polarization networks, the load network, the input matching circuit, as well as access lines, with the blocking capacitors for the connections input and output ports.

H. Stage 7: Fabrication and measurement

Finally, the amplifier is built for measurements in the laboratory. Figure 3 shows photographs of prototype experimental configurations Class-E and Class-F.

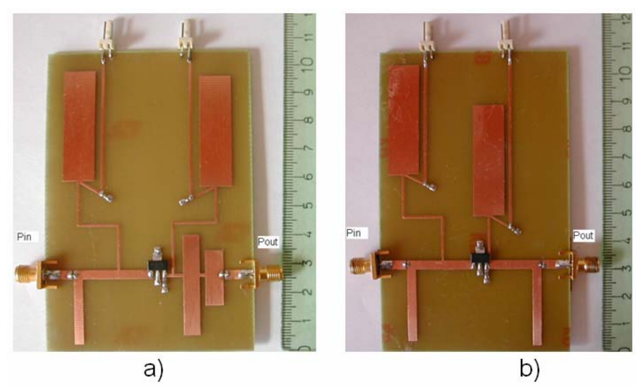

Fig. 3. Experimental prototype of the amplifier. a) Class-E b) Class-F.

To measure the characteristics of the amplifier we use the following instruments: HP 8753D Network Analyzer and Spectrum Analyzer HP 8595E. Performing a scan of input power from 0 to 13 dBm (20 mW) we have obtained the following tables of measurements for amplifiers Class-E and Class-F.

TABLE 1.
OUTPUT POWER CLASS-E AMPLIFIER

Pin (dBm)	Pout (dBm)	Pout (mW)
0	13.75	23.71
2	15.78	37.84
5	18.66	73.45
7	20.3	107.15
10	22.78	189.67
13	25.1	323.59

TABLE 2.
OUTPUT POWER CLASS-F AMPLIFIER

Pin (dBm)	Pout (dBm)	Pout (mW)
0	13.1	20.41
2	15.02	31.76
5	18.0	63.09
7	19.78	95.06
10	21.7	147.91
13	23.1	204.17

The chart shows that for the Class-F amplifier, the output power is lower than for the E-Class, the reason is that it is more difficult to tune and a possible solution is the implementation of an additional adjustment circuit.

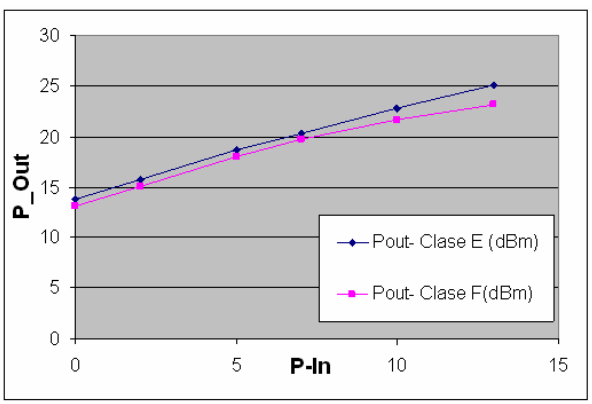

Fig. 4. Output power vs input power in amplifier operation modes Class-E and Class- F

The figure below shows the spectral output power of Class-E and Class-F amplifiers by applying an input of 13 dBm (20 mW) obtained with the spectrum analyzer. The value of power at the operating frequency of 1 GHz is 25.1 dBm (323.59 mW) for the Class-E and 23.1 dBm (204.7 mW) for the Class-F.

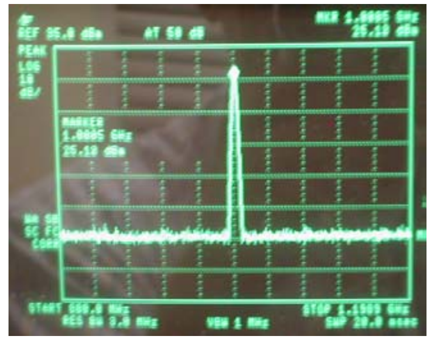

Fig. 4. Spectrum of Class-E power amplifier

The output power is centered at the design frequency of 1 GHz design.

IV. Conclusions

Several studies show that non-linear amplifiers cannot achieve the theoretical efficiency equal to 100% due to non-ideal characteristics of transistors. Active devices have real values of saturation and cutoff voltage and current different from zero; when one of the values tends to zero the other tends to a high value and therefore the product of both values is representative so that the efficiency is affected drastically. As result of the non-ideality of the transistor switch, an overlap occurs between the drain voltage and current. This overlap causes a power dissipation that degrades the efficiency.

Within these non-ideal characteristics the main considerations in the design are the output capacitance, the resistance and the transition frequency.

The present paper described a methodology by which it is done to go from design to manufacture of non-linear power amplifiers for RF, by applying theoretical models and considering the non-ideal characteristics of active devices.

Although a little difficult because of limitations, due to the lack of materials for substrates, in addition to the tight market of electronic components for RF and, just enough instrumentation for the characterization of the devices, power amplifiers can be built using microstrip technology; they can be described in an approximate way to compare the results of these measurements with those of the simulations and to generate some conclusions about the design process.

Finally, with regard to the manufacture, the use of microstrip facilitates the practical implementation of RF power amplifiers. There is a no wide range of values available in the market for lumped elements and that can be replaced easily by microstrip.

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